ABSTRACT OF THE DISCLOSURE

An embodiment of the invention provides a circuit for reducing power in memory cells. The input of the circuit is connected to the wordline of the memory cells. When the wordline is active, the output of the circuit applies a voltage near VDD to the positive voltage supply node of the memory cells. When the wordline is inactive, the output of the circuit applies a voltage that is reduced by at least one V_t from VDD to the positive voltage supply node of the memory cells.